

SHEET 1 OF 11

INFORMATION DISCLOSURE
CITATION IN AN
APPLICATION

(PTO-1449)

ATTY. DOCKET NO.
043876-0144SERIAL NO.
10/616,303APPLICANT
HANSEN, C., et al.FILING DATE
July 10, 2003GROUP
2676

U.S. PATENT DOCUMENTS

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

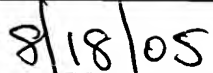
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	L-103	Culler, David E., et al., "Analysis Of Multithreaded Microprocessors Under Multiprogramming", Report No. UCBCSD 921687, May 1992 p.1-17.	
	L-104	James Laudon et al., "Architectural And Implementation Tradeoffs In The Design Of Multiple-Context Processors", CSL-TR-92-523, May 1992 p. 1-24.	
	L-105	Ide, et al., "A 320-MFLOPS CMOS Floating-point Processing Unit for Superscalar Processors," 28 IEEE Custom Integrated Circuits Conference, 1992, p. 30.2.1-30.2.4.	
	L-106	High Speed DRAMs, Special Report, IEEE Spectrum, vol. 29, no. 10, October 1992.	
	L-107	Moyer, Steven A., "Access Ordering Algorithms for a Multicopy Memory," IPC-TR-92-0 1 3, December 18, 1992.	
	L-108	Moyer, Steven A., "Access Ordering and Effective Memory Bandwidth," Ph.D. dissertation, University of Virginia, April 5, 1993.	
	L-109	"Hardware Support for Dynamic Access Ordering: Performance of Some Design Options", Sally McKee, Computer Science Report No. CS-93-08, August 9, 1993.	
	L-110	McGee et al., "Design of a Processor Bus Interface ASIC for the Stream Memory Controller" p. 462-465.	
	L-111	McKee et al., "Experimental Implementation of Dynamic Access Ordering," August 1, 1993, p. 1-10.	
	L-112	McKee et al., Increasing Memory Bandwidth for Vector Computations, Technical Report CS-93-34 August 1, 1993, p.1-18.	
	L-113	Sally A. McKee et al., "Access Order and Memory-Conscious Cache Utilization" Computer Science Report No. CS-94- 10, March 1, 1994, p.1-17.	
HN	L-114	McKee, et. al., "Bounds on Memory Bandwidth in Streamed Computations," Computer Science Report CS-95-32, March 1, 1995.	
EXAMINER <i>Blackly Harestine</i>		DATE CONSIDERED <i>8/18/05</i>	

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1 Applicant's unique citation designation number (optional). 2 Applicant is to place a check mark here if English language Translation is attached.

INFORMATION DISCLOSURE CITATION IN AN APPLICATION (PTO-1449)		ATTY. DOCKET NO. 043876-0144	SERIAL NO. 10/616,303
		APPLICANT HANSEN, C., et al.	
		FILING DATE July 10, 2003	GROUP 2676
OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)			
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	L-115	McKee, Sally A., "Maximizing Memory Bandwidth for Streamed Computations," A Dissertation Presented to the Faculty of the School of Engineering and Applied Science at the University of Virginia, May 1995.	
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	L-117	"Control Data 6400/6500/ 6600 Computer Systems Reference Manuals" 1969 available at http://led-thelen.org/comp-hist/CDC-6600-R-M.html ("CDC 6600 Manuals").	
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	L-128	Yulun Wang, et al, "The 3DP: A processor Architecture for Three-Dimensional Applications, January 1992, p. 25-36.	
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HK	L-129	"IEEE Draft Standard for High-Bandwidth Memory Interface Based on SCI Signaling Technology (RamLink)", 1995, pp.1-104, IEEE.	
	L-130	Gerry Kane and Joe Heinrich, "MIPS RISC Architecture" 1992, Publisher: Prentice-Hall Inc., A Simon & Shuster Company, Upper Saddle River New Jersey.	
	L-131	CATHY MAY et al. "The Power PC Architecture: A Specification For A New Family of Risc Processors" Second Edition May 1994, pp. 1—518, Morgan Kaufmann Publishers, Inc. San Francisco CA, IBM International Business Machines, Inc.	
	L-132	"IEEE Standard for Scalable Coherent Interface (SCI)", Published by the Institute of Electrical and Electronics Engineers, Inc. August 2, 2003, pp. 1-248.	
	L-133	DON TOLMIE and Don Flanagan, "HIPPI: It's Not Just for Supercomputers Anymore" Data Communications published May 8, 1995.	
	L-134	Kevin D. Kissell "The Dead Supercomputer Society The Passing Of A Golden Age", February, 1998 pp. 1-2, [http://www.paralogos.com/DeadSuper].	
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	L-137	JOE HEINRICH, "MIPS R4000 Microprocessor User's Manual Second Edition" 1994 MIPS Technologies, Inc. pp. 1-754.	
	L-138	Litigation proceedings in the matter of <i>Microunity Systems Engineering, Inc. v. Dell, Inc. et al.</i> , Corrected Preliminary Invalidity Contentions and Exhibits, filed January 12, 2005, Civil Action No. 2:04-CV-120(TJW), U.S. District Court for the Eastern District of Texas Marshall Division.	
	L-139	Ang, StarT Next Generation: Integrating Global Caches and Dataflow Architecture, Proceedings of the ISCA 1992.	
	L-140	Saturn Architecture Specification, published April 29, 1993.	
	L-141	C4/XA Architecture Overview, Convex Technical Marketing presentation dated November 11, 1993 and February 4, 1994.	
	L-142	Convex 3400 Supercomputer System Overview, published July 24, 1991.	
	L-143	Giloi, Parallel Programming Models and Their Interdependence with Parallel Architectures, IEEE Proceedings published September 1993.	
HK	L-144	PCT International Search Report and Written Opinion dated March 11, 2005, corresponding to PCT/US04/22126	
HK	L-145	Supplementary European Search Report dated March 18, 2005, corresponding to Application No. 96928129.4	
EXAMINER <i>Nackly Honestine</i>		DATE CONSIDERED 8/18/05	

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Examiner's consideration of the same. Furthermore, the attached form PTO-1449 includes citations to some materials for which it is difficult to obtain additional copies. In view of the Petition and in the interests of efficiency, Applicants' respectfully request that a copy of each of the cited documents be made of record in the present application.

This Information Disclosure Statement is being filed within three months of the U.S. filing date OR before the mailing date of a first Office Action on the merits. No certification or fee is required.

Applicants bring to the Examiner's attention the following pending applications of Craig C. Hansen et al., which may include subject matter related to the present application:

Application Number	Title
10/418,113	Multiplier Array Processing System With Enhanced Utilization At Lower Precision
10/436,340	System With Wide Operand Architecture, And Method
10/646,787	Method And Software For Partitioned Group Element Selection Operation
10/705,946	Programmable Processor And Method For Partitioned Group Shift
10/712,430	System And Software For Catenated Group Shift Instruction
10/716,561	Programmable Processor And Method For Matched Aligned And Unaligned Storage Instructions
10/716,568	System And Software For Matched Aligned And Unaligned Storage Instructions
10/757,515	Method And Software For Multithreaded Processor With Partitioned Operations
10/757,516	Programmable Processor And System For Store Multiplex Operation
10/757,524	Programmable Processor And For Partitioned Group Element Selection Operation
10/757,836	Programmable Processor And System For Partitioned Floating-Point Multiply-Add Operation.

10/616,303

<i>MM</i>	10/757,851	Method And Software For Partitioned Floating-Point Multiply-Add Operations
	10/757,866	Method And Software For Store Multiplex Operation
	10/757,925	Method And Software For Partitioned Group Element Selection Operation
<i>MM</i>	10/757,939	Multithreaded Programmable Processor And System With Partitioned Operations


The attached form PTO-1449 includes (but is not exclusively limited to) documents that were cited in on-going litigation proceedings between the assignee of the present application, Dell Inc. and Intel Corp. (U.S. District Court for the Eastern District of Texas, Marshall Division (Civil Action No. 2:04-CV-120(TJW))). This litigation involves seven patents that are in the same family as each of the above applications.

Additionally, some documents were cited in related foreign applications. A copy of the foreign search report or office action is attached for the Examiner's information.

Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

McDERMOTT WILL & EMERY LLP



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